PERIPHERAL COMPONENT INTERCONNECT ARBITER IMPLEMENTATION WITH DYNAMIC PRIORITY SCHEME

Sujith Arramreddy
Ragu Appanagari

ABSTRACT OF THE INVENTION

A dynamic priority scheme is provided that uses information including the status of the target and data availability in deciding which PCI master should be assigned ownership of the bus. The target uses delayed transactions to complete a read access targeted to it. The target also integrates a buffer management scheme, in one embodiment an input/output cache, for buffer management. The present invention optimizes the performance and utilization of the PCI bus.